REDUCED PESSIMISM CLOCK GATING TESTS FOR A TIMING ANALYSIS TOOL

ABSTRACT

A method for analyzing a gated clock design in which a disabling clock gating transition prevents an output transition from occurring, assuring that no clock glitching occurs. Delays and slews are computed so that the arrival time computation that includes clock and gate signal delays are computed at the output, providing tests which ensure that no glitch situation occurs. The delays and slews are computed using a static timing analysis, which includes situations such as a late and early arriving gate clock signals. The invention may be used in any static timing analysis test to ensure that a first transition on one input of a circuit prevents the propagation of a second transition on another input of the circuit.